Electrical TCAD Simulations of a Germanium pMOSFET Technology

Geert Hellings, *Student Member, IEEE*, Geert Eneman, Raymond Krom, Brice De Jaeger, Jérôme Mitard, An De Keersgieter, Thomas Hoffmann, Marc Meuris, and Kristin De Meyer, *Senior Member, IEEE*

***Abstract*—A commercial technology computer-aided design device simulator was extended to allow electrical simulations of sub-100-nm germanium pMOSFETs. Parameters for generation/recombination mechanisms (Shockley–Read–Hall, trap-assisted tunneling, and band-to-band tunneling) and mobility models (impurity scattering and mobility reduction at high lateral and transversal field) are provided. The simulations were found to correspond well with the experimental I–V data on our Ge transistors at gate lengths down to 70 nm and various bias conditions. The effect of changes in halo dose and extension energies is discussed, illustrating that the set of models presented in this paper can prove useful to optimize and predict the performance of new Ge-based devices.**

***Index Terms*—Germanium, modeling, MOSFET, technology computer-aided design (TCAD) simulations.**

I. Introduction

As SCALING of CMOS becomes increasingly more difficult, other materials have been considered to replace Si as the channel material. Because of its high electron (3900 $cm^2/V \cdot s$) and hole (1900 $cm^2/V \cdot s$) mobilities, germanium has been widely investigated in recent years [1], [2]. The progress made in the electrical passivation of the interface between the germanium channel and the gate dielectric has resulted in Ge pMOS devices with gate lengths well below 100 nm [3], [4]. Technology computer-aided design (TCAD) software is widely used to optimize and predict the electrical behavior of new devices. Still, several physical models or their parameters, which are indispensable for sub-100-nm MOSFET simulations in germanium, are not generally available in commercial software at this time.

Therefore, in this paper, we extend a commercial TCAD device simulator (sdevice [5]) by adding a consistent parameter set based on the experimental results from Ge devices. Comparing with electrical results from Ge p-channel field-effect transistors (pFETs) with different gate lengths and implant conditions allows the use of these models and their parameters for reliable device simulations.

This paper is structured as follows. Section II outlines the processing details of the Ge pMOS devices used in this paper. Section III provides the physical models and details on how their parameters are determined using experimental data on junction leakage and high- and low-field mobilities. Finally, in Section IV, the TCAD model proposed in Section III is compared to experimental measurements in IMEC's Ge pFETs. The TCAD calibration strategy is shown schematically in Fig. 1.

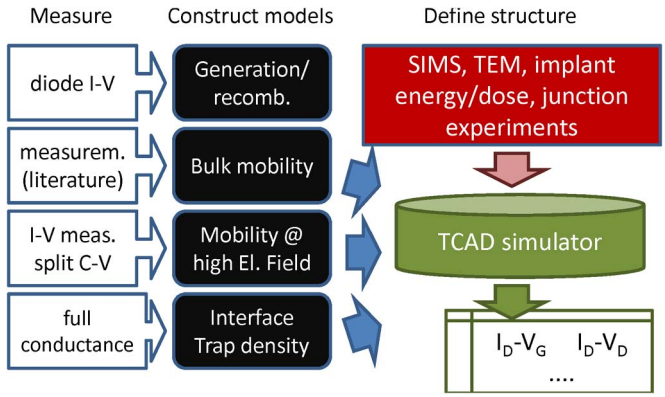

Fig. 1. Flowchart illustrating the TCAD calibration strategy used in this paper; the electrical models and the device structure are defined starting from various measurement techniques.

II. Experimental Setup

PMOS devices were fabricated using a Si-compatible process flow on 200-mm (100)-oriented Si wafers with a relaxed epitaxial Ge layer supplied by ASM. The top Ge layer has a thickness of 1.5 μm and a threading dislocation density of 2×10^7 cm^{-2}. The wafers received a phosphorus channel doping up to a concentration of 3×10^{17} cm^{-3}, followed by deposited SiO_2 isolation. The gate stack consists of an ultrathin partially oxidized Si layer [6], 4-nm HfO_2, and a 10-nm-TiN/80-nm-TaN metal gate. After this, arsenic halos are implanted at an energy of 80 keV and different doses, followed by the extension (or LDD) boron implant (2 or 2.4 keV; 8×10^{14} cm^{-2}). This is followed by the spacer definition and boron HDD implants. The activation anneal is carried out in N_2 atmosphere at 550 °C for 5 min, resulting in negligible dopant diffusion under the current conditions [1]. Finally, a NiGe contact is made to the germanium by annealing 5 nm of deposited Ni in a two-step

Manuscript received May 6, 2010; revised July 7, 2010; accepted July 10, 2010. Date of publication August 12, 2010; date of current version September 22, 2010. This work was supported in part by the European Commission under DualLogic Project 214579. The work of G. Hellings was supported by a Ph.D. grant from the Institute for the Promotion of Innovation through Science and Technology in Flanders (IWT-Vlaanderen), Brussels, Belgium. The work of G. Eneman as a Post-Doctoral Fellow was supported by the Fund for Scientific Research, Brussels, Belgium. The review of this paper was arranged by Editor V. R. Rao.

G. Hellings, G. Eneman, R. Krom, and K. De Meyer are with imec, 3001 Leuven, Belgium, and also with the Department of Electrical Engineering, University of Leuven, 3001 Leuven, Belgium.

B. De Jaeger, J. Mitard, A. De Keersgieter, T. Hoffmann, and M. Meuris are with imec, 3001 Leuven, Belgium.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TED.2010.2060726

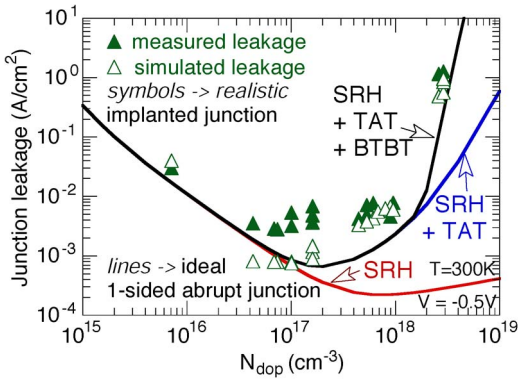

Fig. 2. (Empty symbols) Measured and (solid symbols) simulated leakage for various p+/n junctions with different implant conditions in Ge, taking into account the models for SRH, TAT, and BTBT. The lines plot the simulated leakage for an ideal abrupt one-sided junction as a function of counterdoping.

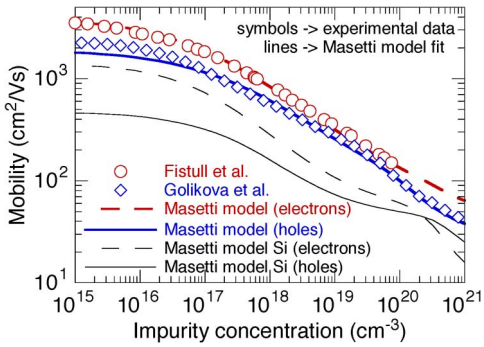

Fig. 3. Measured bulk mobility for electrons and holes in germanium from literature and the fitted relationships with the Masetti model used in this paper (Si relationship is also included).

rapid thermal processing flow [1]. The process is concluded by TiN/Ti/Al/TiN back-end processing.

III. TCAD Models

In this section, we present the different physical models that were used to simulate Ge pMOSFET devices. Since these may be implemented in any device simulator, the actual implementation and model parameters (specific for Sentaurus sdevice) have been moved to the Appendix. Some basic models (e.g., bandgap and density of states) are not mentioned in this section; their parameters were left unchanged from the defaults.

A. Generation–Recombination Mechanisms

The small bandgap of germanium (0.66 eV) is known to result in higher junction leakage [7], [8] compared to that in silicon devices. For this reason, an implementation of the various recombination mechanisms is indispensable for simulations of advanced Ge technologies.

1) SRH: The Shockley–Read–Hall (SRH) model describes recombination through deep-level defects in the bandgap. Typically, a description is used in terms of minority carrier lifetimes (τ_n and τ_p), dependent on the local defect concentration. The parameters for this model were chosen to achieve a good agreement with published measurements of the minority carrier lifetime [9] and our own experimental leakage measurements on p+/n junctions [8]. It should be noted that the lifetimes reported in [9] are slightly higher than what would fit with our experimental data. This may be due to the differences in sample morphology and remaining defects. For the position of the trap level in the bandgap, a midgap energy level is assumed (0.33 eV for Ge), as in the Si case.

2) TAT: In large electric fields, the lifetime of the minority carriers is reduced through the mechanism of trap-assisted tunneling (TAT). This is relevant when simulating the abrupt junctions in scaled transistors. The model proposed by Hurkx *et al.* [10] to describe TAT was included in our simulations. Its description in terms of a reduced field-dependent carrier lifetime in the presence of TAT $[\tau_{\mathrm{TAT}} = \tau_{\mathrm{SRH}}/(1+\Gamma)]$ has shown good agreement with leakage measurements on our p+/n junctions [8].

3) BTBT: In even higher electric fields, the junction leakage is further increased through phonon-assisted band-to-band tunneling (BTBT). The model proposed by Schenk *et al.* [11] provides a simplified formalism for the purpose of device simulations: The generation/recombination rate is a function of the ratio of the local electric field F in the structure and a critical electric field $F_c^{\pm}$ given by [5]

$$F_c^{\pm} = B(E_{g,\mathrm{eff}} \pm \hbar\omega)^{3/2}.$$

This formula contains the bandgap of the material and a prefactor B containing the effective mass for tunneling. For Ge, this prefactor was scaled with respect to its Si default value, based on the ratio of the effective masses in both materials.

4) Generation–Recombination—Experimental Procedure: To check the applicability of the models discussed earlier in simulations of scaled Ge pMOS devices, the junction leakage was measured for various p+/n junctions. At the same time, the dopant profiles were simulated based on the implant conditions using a Monte Carlo implant simulator (calibrated for Ge—taurusMC [12]). The dopant profile, as well as the total impurity profiles, was then fed to the device simulator. This approach allows simulating the leakage for these junctions, taking implant tails and the local impurity concentration into account. In this manner, pairs of measured and simulated junction leakages are obtained (empty and solid symbols, respectively) in Fig. 2, where the result of this calibration is depicted graphically.

To illustrate the contribution of the different leakage mechanisms (SRH, TAT, and BTBT) as a function of active doping concentration at the p+/n junction, ideal one-sided junctions were simulated as well, activating the different leakage mechanisms progressively. This results in three lines in Fig. 2, each considering the different leakage mechanisms. It can be seen that the TAT mechanism should be included when dealing with doping concentrations above 10^{17} cm^{-3} and that the BTBT mechanism is dominant for doping concentrations in excess of 2×10^{18} cm^{-3}. Both of them are typically present in sub-100-nm Ge devices (in HDD and extension junctions, respectively).

B. Mobility

The second set of models is related to carrier mobility. Germanium has a higher bulk hole mobility than silicon. This is

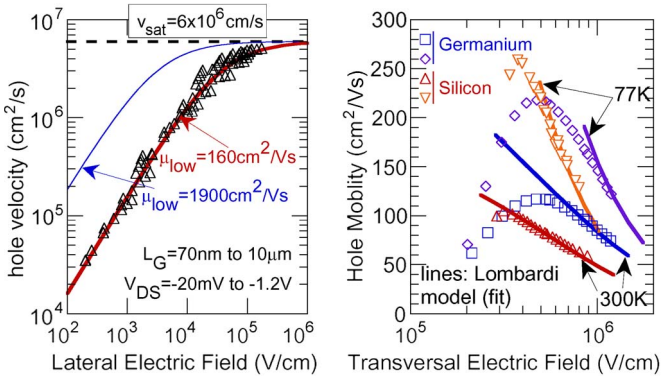

Fig. 4. (Left) Measured average hole velocity in Ge pMOSFETs with L_G's ranging from 70 nm to 10 μm as a function of average lateral electric field in the channel and theoretical fit for this relationship using the formula from [13] ($\beta = 1$ and $\mu_{\rm low} = 1900$ and 160 cm^2/V $\cdot$ s). (Right) Extracted hole inversion layer mobility as a function of transversal electric field at 77 K and 300 K for Si and Ge, respectively, and the fits used in this paper using the enhanced Lombardi model [14].

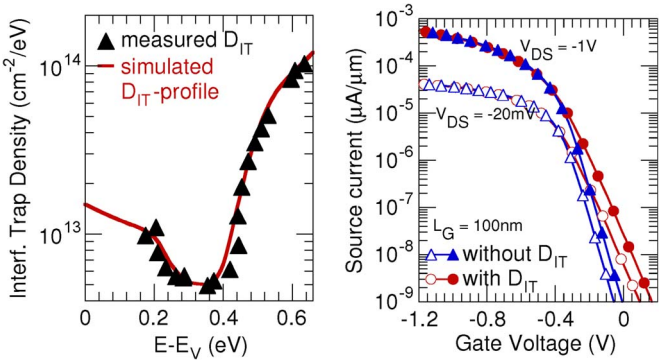

Fig. 5. (Left) Measured interface trap density as a function of energy (extracted with the full-conductance method) for the Ge passivation recipe used in this paper and (lines) the profile used for the simulations in this paper. (Right) Simulated drain current as a function of V_G with and without interface traps, showing improved short-channel control in the device without interface traps (discussed in Section IV-C).

undoubtedly the main driver behind the renewed interest in Ge as a channel material for high-performance logic applications. However, when considering the carrier transport in a scaled Ge MOSFET, this argument becomes inevitably more complex because of the high transversal and lateral electric fields. In this paragraph, we attempt to present a consistent set of models that should allow performing TCAD simulations of sub-100-nm Ge pMOS devices. Also, for this section, the model parameters are included in the Appendix.

1) Phonon Scattering: The basic mobility model accounts only for phonon scattering. Since the higher Ge bulk mobility for both electrons (3900 versus 1400 cm^2/V $\cdot$ s) and holes (1900 versus 470 cm^2/V $\cdot$ s) is already included in the default parameter set, it is not discussed further here.

2) Impurity Scattering: In doped semiconductors, the scattering of carriers by impurity ions results in a degradation of carrier mobility. The model used here was proposed by Masetti *et al.* [15] and is suited for indirect semiconductors. In germanium, the doping-dependent mobility was measured for electrons and holes by Fistul *et al.* [16] and Golikova *et al.* [17], respectively. The parameters of the Masetti model were modified from the Si defaults to achieve an empirical fit with their experimental Ge data, which is shown in Fig. 3. Notably, as can also be seen in Fig. 3, the mobility of Ge remains higher than that of Si, even at higher impurity concentrations.

3) Velocity Saturation: In high lateral electric fields, the carrier drift velocity is not proportional anymore to the electric field. Instead, the carrier velocity saturates at a material and carrier-dependent speed $v_{\rm sat}$. Various sources state a numerical value of $v_{\rm sat}$ around 6×10^6 cm/s for both electrons and holes in Ge [18]–[20]. However, this is a bulk material property. The average hole velocity in the inversion layer was extracted from I–V measurements for our Ge pMOSFETs using the method described in [21] (gate lengths ranging from 70 nm to 10 μm and $V_{\rm DS} = -20$ mV to -1.2 V) and found to be in good agreement with the expression from [13]

$$v = \frac{\mu_{\rm low} E}{[1 + (\mu_{\rm low} E / v_{\rm sat})^{\beta}]^{1/\beta}}$$

where $\mu_{\rm low}$ is the low field mobility, E is the electric field, and β is a fitting parameter. Good agreement was found for $\mu_{\rm low} = 160$ cm^2/V $\cdot$ s, assuming $\beta = 1$ as for holes in silicon.

4) Acoustic Phonon/Surface Roughness Scattering: In the inversion layer of a MOSFET, the carriers are attracted to the semiconductor–dielectric interface by the large transversal (vertical) electric field. This extra scattering is dominated by acoustic phonon scattering at medium electric fields and by surface roughness scattering at high electric fields. Additionally, the acoustic phonon scattering is very sensitive to temperature, while the scattering due to surface roughness is temperature independent [22].

For this reason, we have extracted the hole mobility at 77 K and 300 K on our Ge pFETs and on Si reference devices [23], respectively. Because of the temperature-dependent hole mobility measurements, the two degradation mechanisms can be separated. These were then described in terms of the enhanced Lombardi model that is available in sdevice and based on [14]. The result of this exercise is given in Fig. 4(b). We found that a satisfactory fit could be obtained in the presence of a high transversal electric field by tuning the parameters of the enhanced Lombardi model. Note that this model does not include the Coulomb scattering component that is dominant at low transversal electric field.

C. Interface Traps

The electrical passivation of the interface between the high-κ dielectric and the channel is a key challenge for Ge technology. A high density of active interface traps will severely harm the performance of any Ge MOSFET. Various attempts have been made to find a process scheme that results in such a passivation, and promising results have been obtained with (among others) an ultrathin Si layer [6] and GeO$_x$ [24], [25].

In this paper, we will focus on pMOSFETs with an ultrathin Si passivation layer. For this processing scheme, the density of interface traps as a function of energy in the bandgap was extracted with the full-conductance method [26]. The extracted profile of interface traps was included in our TCAD simulations. Fig. 5(a) shows the measured data points for a

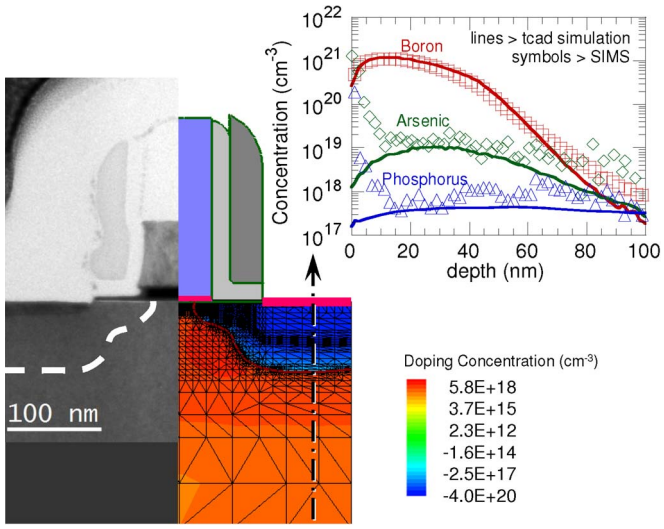

Fig. 6. (Left) TEM image of the $L_G = 70$-nm Ge pMOS and the simulated structure, showing dopant profiles and meshing. (Right) Measured (SIMS) and simulated chemical concentration of B, P, and As in the HDD region of this device.

deposited Si layer of 8 ML and the continuous profile used in simulations.

IV. Simulation Results

In this section, the models earlier will be used in electrical simulations of our Ge pMOS devices. Three separate items will be discussed. First, simulated drain, source, and bulk currents as a function of V_G and V_D are compared with electrical measurements on our Ge pMOS devices with gate lengths (L_G's) ranging from 70 nm to 1 μm. Second, the effect of changes in halo and extension (LDD) energies on short-channel effects and drain-to-bulk leakage is investigated. Finally, it is shown that a pMOSFET without the modeled interface traps has a steeper subthreshold slope.

Since such electrical simulations are quite sensitive to the dopant profiles of the simulated device, these were simulated with the calibrated Monte Carlo implant simulator mentioned previously. The result of these implant simulations and numerical meshing is shown in Fig. 6(a), together with a transmission electron microscopy (TEM) image of the 70-nm device. A 1-D secondary ion mass spectrometry (SIMS) measurement of the HDD region of the device shows the simulated and measured chemical dopant concentrations for boron, the arsenic halo, and the phosphorus well. The noise on the measured As profile is quite large, which is due to mass interference during the SIMS measurement. Note that ion channeling during the implant is taken into account by the simulator and is quite pronounced for the boron profile.

Based on [27], the B junctions are assumed not to diffuse during rapid thermal anneal, and the maximum active B concentration for the extensions was set to 4×10^{20} cm^{-3}.

A. I_D–V_G and I_D–V_D Simulations

The set of models discussed before can be used to perform electrical simulations of our Ge pMOS devices. In Fig. 7(a), (c), (e), and (f), the simulated currents are plotted together with

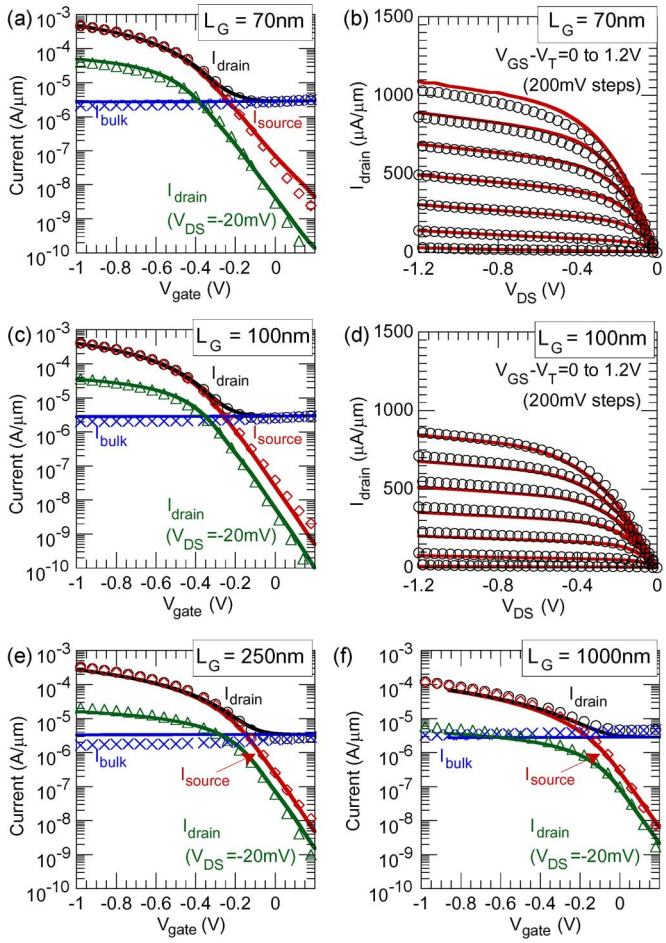

Fig. 7. (Symbols) Measured and (lines) simulated drain, source, and substrate currents as a function of V_G for Ge pMOS devices with $L_G = 70$ nm–1 μm at $V_{\rm DS} = -20$ and -1 V and as a function of V_D for devices with $L_G = 70$ and 100 nm for $V_{\rm GS} - V_T = 0$ to -1.2 V.

those measured on a representative device as a function of V_G for $V_{\rm DS} = -20$ mV and -1 V and $L_G = 70$, 100, 250, and 1000 nm, respectively. The simulated I_D–V_D current is shown in Fig 7(b) and (d), together with the measured one for $V_{\rm GS}$–V_T ranging from 0 to -1.2 V for the two shortest devices. The simulated curves show a reasonable agreement with the measured ones, e.g., for the 70-nm device at $V_{\rm GS} - V_T = V_D = -1$ V, a drain current of 830 μA/μm is observed (simulated: 860 μA/μm), while a drain-induced barrier-lowering (DIBL) value of 140 mV/V is comparable to the simulated 130 mV/V. The drain-to-bulk junction leakage is also reproduced (e.g., 2.24×10^{-6} A/μm (measured) versus 2.79×10^{-6} A/μm (simulated) for $L_G = 70$ nm).

The mobility models at high lateral and transversal electric fields (Sections III-B-3 and III-B-4) are indispensable in obtaining a good agreement between the simulated and measured drive currents and are observed to be sufficient for L_G down to 70 nm. For even smaller devices, the phenomenon of velocity overshoot, which is predicted by Monte Carlo simulations [28], might have to be included as well. In turn, the generation/recombination models from Section III-A are needed to capture the high drain-to-bulk leakage and (to a certain extent) gate-induced drain leakage.

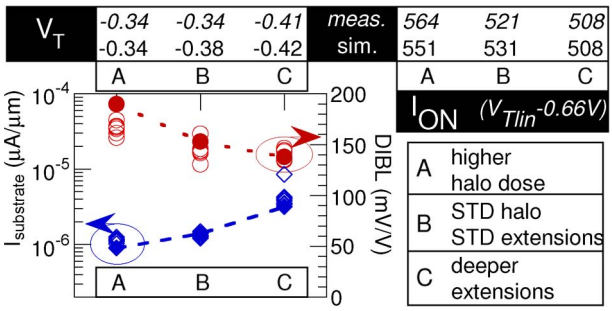

Fig. 8. (Empty symbols) Measured and (full symbols) simulated drain-to-substrate leakage and DIBL for (B) the standard Ge pMOS device with $L_G =$ 70 nm (graph) and (A and C) the effect process variations. The measured (median) and simulated threshold voltage and drive current ($V_D = -1$ V) are printed in the table.

B. Alternative Implant Conditions

Since TCAD software is often used to optimize and predict the electrical effect of any change in the processing scheme, the validity of such an extrapolation has to be closely monitored. Here, an example case is presented, evaluating the effect of two perturbations to our standard transistor flow: 1) increasing the extension implant energy from 2 to 2.4 keV and 2) increasing the implanted halo dose from 5×10^{13} to 6.5×10^{13} cm^{-2}.

From the simulated, as well as from the measured, I–V curves on such devices, $I_{\rm ON}$, V_T, DIBL, and drain-to-bulk junction leakage were extracted. This comparison is shown in Fig. 8, where these quantities are compared for our standard flow (condition B) and for the perturbations (A and C). Comparing the measured quantities with the simulated ones shows that the electrical effect of these processing changes can be predicted by the simulator. First, increasing the extension junction depth results in reduced short-channel control (higher DIBL) and lower drain-to-bulk leakage since that junction becomes less abrupt (not shown). Second, increasing the halo dose results, as expected, in improved short-channel control (lower DIBL), higher drain-to-bulk leakage, and lower $I_{\rm ON}$.

C. Modeling of Interface Traps

In this third part, the effect of interface traps is illustrated. In the previous simulations, the trap spectrum ($D_{\rm IT}$), measured with the full-conductance method, was included (see Section III-C). Obviously, this spectrum is specific to the passivation process available at this moment. This raises the question what the characteristics would be of a hypothetical Ge pMOSFET without interface traps. For this reason, the 100-nm gate-length Ge pMOS was simulated also without these interface traps, keeping all other models unchanged. As can be seen in Fig. 5(b), the interface traps have a visible effect on the transistor's switching characteristics. Notably, removing them reduces DIBL from 90 to 58 mV/V and the subthreshold slope from 120 to 80 mV/dec. As such, further reducing the interface trap density is necessary to obtain a better electrostatic gate control. Additionally, the dependence of carrier mobility on transversal electric field can be expected to be different. As such, the drive current should increase as the interface quality improves.

TABLE I
SRH RECOMBINATION (Sharfetter)

parameter	units	**Si** (e,h)	**Ge** (e,h)
tau$_{min}$	s	0, 0	0, 0
tau$_{max}$	s	1×10^{-5}, 3×10^{-6}	4×10^{-5}, 4×10^{-5}
N$_{ref}$	cm^{-3}	10^{16}, 10^{16}	10^{14}, 10^{14}
γ	-	1, 1	0.85, 0.85
T$_\alpha$	-	-1.5, -1.5	-1.5, -1.5
T$_{coeff}$	-	2.55, 2.55	2.55, 2.55
E$_{trap}$	eV	0.0, 0.0	0.0, 0.0

TABLE II
TAT (HurckxTrapAssistedTunneling)

parameter	units	**Si** (e,h)	**Ge** (e,h)
m$_t$	-	0.5, 0.5	0.12, 0.34

TABLE III
BTBT (Band2BandTunneling)

parameter	units	Si	Ge
A	cm s^{-1} V^{-2}	8.977×10^{20}	8.977×10^{20}
B	eV$^{-3/2}$ V cm^{-1}	2.147×10^{7}	1.6×10^{7}

TABLE IV
PHONON SCATTERING (ConstantMobility)

parameter	units	**Si** (e,h)	**Ge** (e,h)
μ_{max}	cm^{2}V^{-1}s^{-1}	1417, 470.5	3900, 1900
exponent	-	2.5, 2.2	2.5, 2.2

V. SUMMARY AND CONCLUSION

In summary, a commercial TCAD device simulator has been extended by adding a consistent parameter set, which is applicable to Ge pMOSFET device simulations. The model parameters for generation/recombination mechanisms (SRH, TAT, and BTBT) and mobility models (impurity scattering and mobility reduction at high lateral and transversal fields) have been adapted based on available experimental data. The electrical simulations of Ge pMOS devices using these models and parameters have been found to be in good agreement with the measured I–V curves for our devices for various bias conditions and gate lengths ranging from 70 nm to 1 μm. Finally, the effect of changes in halo dose and extension energies has been simulated and shown to be in good agreement with the experimental results. The set of models presented in this paper can prove useful to optimize and predict the performance of new Ge-based devices.

APPENDIX
SIMULATION PARAMETERS

This Appendix contains the model parameters used in this paper. Each time, both the name of the physical phenomenon and the name of the parameter set are given (e.g., SRH recombination is modeled using the Scharfetter data set in sdevice) together with the default silicon values. If different values apply for electrons and holes, both values are given in this order, separated by a comma.

A) Recombination: See Tables I–III.

B) Mobility: See Tables IV–VII.

TABLE V
IMPURITY SCATTERING (DopingDependence)

param.	units	**Si** (e,h)	**Ge** (e,h)
μ_{min1}	cm^2/Vs	52.2, 44.9	60, 60
μ_{min2}	cm^2/Vs	52.2, 0.0	0, 0
μ_1	cm^2/Vs	43.4, 29	20, 40
P_c	cm^{-3}	0, 9.23×10^{16}	10^{17}, 9.23×10^{16}
C_r	cm^{-3}	9.68×10^{16}, 2.23×10^{17}	8×10^{16}, 2×10^{17}
C_s	cm^{-3}	3.34×10^{20}, 6.10×10^{20}	3.43×10^{20}, 10^{20}
α	-	0.68, 0.719	0.55, 0.55
β	-	2.0, 2.0	2.0, 2.0

TABLE VI
HIGH LATERAL FIELD MOBILITY (HighFieldDependence)

param.	units	**Si** (e,h)	**Ge** (e,h)
v_{sat0}	cm/s	1.07×10^7 , 8.37×10^6	6×10^6 , 6×10^6

TABLE VII
HIGH TRANSVERSAL FIELD MOBILITY [EnormalDependence (Holes Only)]

param.	units	Si	Ge
B	cm/s	9.925×10^6	1.993×10^5
C	$cm^{5/3}V^{-2/3}s^{-1}$	2.947×10^3	4.875×10^3
N_0	cm^{-3}	1	1
λ	-	0.0317	0.0317
k	-	1	1
δ	cm^2/Vs	2.0546×10^{14}	1.705×10^{11}
A	-	2	1.5
$\alpha_\perp$	cm^3	0	0
N_1	cm^{-3}	1	1
ν	-	1	1
η	$V^2cm^{-1}s^{-1}$	2.0546×10^{30}	2.0546×10^{30}
l_{crit}	cm	10^{-6}	10^{-6}

ACKNOWLEDGMENT

The authors would like to thank the IMEC core partners within IMEC's Industrial Affiliation Program on Logic/Ge-III/V.

REFERENCES

[1] D. Brunco, B. De Jaeger, G. Eneman, J. Mitard, G. Hellings, A. Satta, V. Terzieva, L. Souriau, F. Leys, G. Pourtois, M. Houssa, G. Winderickx, E. Vrancken, S. Sioncke, K. Opsomer, G. Nicholas, M. Caymax, A. Stesmans, J. Van Steenbergen, P. Mertens, M. Meuris, and M. Heyns, "Germanium MOSFET devices: Advances in materials understanding, process development, and electrical performance," *J. Electrochem. Soc.*, vol. 155, no. 7, pp. H552–H561, 2008.

[2] K. C. Saraswat, C. O. Chui, T. Krishnamohan, A. Nayfeh, and P. McIntyre, "Ge based high performance nanoscale MOSFETs," *Microelectron. Eng.*, vol. 80, pp. 15–21, Jun. 2005, 14th biennial Conference on Insulating Films on Semiconductors.

[3] E. Batail, S. Monfray, C. Tabone, O. Kermarrec, J. Damlencourt, P. Gautier, G. Rabille, C. Arvet, N. Loubet, Y. Campidelli, J. Hartmann, A. Pouydebasque, V. Delaye, C. Le Royer, G. Ghibaudo, T. Skotnicki, and S. Deleonibus, "Localized ultra-thin GeOI: An innovative approach to germanium channel MOSFETs on bulk Si substrates," in *IEDM Tech. Dig.*, Dec. 2008, pp. 1–4.

[4] G. Hellings, J. Mitard, G. Eneman, B. De Jaeger, D. Brunco, D. Shamiryan, T. Vandeweyer, M. Meuris, M. Heyns, and K. De Meyer, "High performance 70-nm germanium pMOSFETs with boron LDD implants," *IEEE Electron Device Lett.*, vol. 30, no. 1, pp. 88–90, Jan. 2009.

[5] Synopsys, Inc., Mountain View, CA, C-2009.06 ed. Sentaurus Device Reference Manual, 2009.

[6] B. De Jaeger, R. Bonzom, F. Leys, O. Richard, J. Van Steenbergen, G. Winderickx, E. Van Moorhem, G. Raskin, F. Letertre, T. Billon, M. Meuris, and M. Heyns, "Optimisation of a thin epitaxial Si layer as Ge passivation layer to demonstrate deep sub-micron n- and p-FETs on Ge-on-insulator substrates," *Microelectron. Eng.*, vol. 80, pp. 26–29, Jun. 2005, 14th biennial Conference on Insulating Films on Semiconductors.

[7] G. Eneman, B. De Jaeger, E. Simoen, D. Brunco, G. Hellings, J. Mitard, K. De Meyer, M. Meuris, and M. Heyns, "Quantification of drain extension leakage in a scaled bulk germanium pMOS technology," *IEEE Trans. Electron Devices*, vol. 56, no. 12, pp. 3115–3122, Dec. 2009.

[8] G. Eneman, M. Wiot, A. Brugere, O. Casain, S. Sonde, D. Brunco, B. De Jaeger, A. Satta, G. Hellings, K. De Meyer, C. Claeys, M. Meuris, M. Heyns, and E. Simoen, "Impact of donor concentration, electric field, and temperature effects on the leakage current in germanium p+/n junctions," *IEEE Trans. Electron Devices*, vol. 55, no. 9, pp. 2287–2296, Sep. 2008.

[9] E. Gaubas, M. Bauza, A. Uleckas, and J. Vanhellemont, "Carrier lifetime studies in Ge using microwave and infrared light techniques," *Mater. Sci. Semicond. Process.*, vol. 9, no. 4/5, pp. 781–787, Aug.–Oct. 2006.

[10] G. Hurkx, D. Klaassen, and M. Knuvers, "A new recombination model for device simulation including tunneling," *IEEE Trans. Electron Devices*, vol. 39, no. 2, pp. 331–338, Feb. 1992.

[11] A. Schenk, "Rigorous theory and simplified model of the band-to-band tunneling in silicon," *Solid State Electron.*, vol. 36, no. 1, pp. 19–34, Jan. 1993.

[12] Synopsys, Inc., Mountain View, CA, C-2009.06 ed. Sentaurus Process Reference Manual, 2009.

[13] D. Caughey and R. Thomas, "Carrier mobilities in silicon empirically related to doping and field," *Proc. IEEE*, vol. 55, no. 12, pp. 2192–2193, Dec. 1967.

[14] C. Lombardi, S. Manzini, A. Saporito, and M. Vanzi, "A physically based mobility model for numerical simulation of nonplanar devices," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 7, no. 11, pp. 1164–1171, Nov. 1988.

[15] G. Masetti, M. Severi, and S. Solmi, "Modeling of carrier mobility against carrier concentration in arsenic-, phosphorus-, and boron-doped silicon," *IEEE Trans. Electron Devices*, vol. ED-30, no. 7, pp. 764–769, Jul. 1983.

[16] V. I. Fistul, M. I. Iglitsyn, and E. M. Omelyanovskii, "Mobility of electrons in germanium strongly doped with arsenic," *Sov. Phys.—Solid State*, vol. 4, no. 4, pp. 784–785, 1962.

[17] O. Golikova, B. Moizhes, and L. Stil'bans, "Hole mobility of germanium as a function of concentration and temperature," *Sov. Phys.—Solid State*, vol. 3, no. 10, pp. 2259–2265, 1962.

[18] E. J. Ryder, "Mobility of holes and electrons in high electric fields," *Phys. Rev.*, vol. 90, no. 5, pp. 766–769, Jun. 1953.

[19] R. D. Larrabee, "Drift velocity saturation in p-type germanium," *J. Appl. Phys.*, vol. 30, no. 6, pp. 857–859, Jun. 1959.

[20] S. M. Sze, *Physics of Semiconductor Devices*. Hoboken, NJ: Wiley, 1981.

[21] L. Trojman, L. Pantisano, M. Dehan, I. Ferain, S. Severi, H. E. Maes, and G. Groeseneken, "Velocity and mobility investigation in 1-nm-EOT HfSiON on Si (110) and (100)—Does the dielectric quality matter?" *IEEE Trans. Electron Devices*, vol. 56, no. 12, pp. 3009–3017, Dec. 2009.

[22] S. Takagi, A. Toriumi, M. Iwase, and H. Tango, "On the universality of inversion layer mobility in Si MOSFETs: Part I—Effects of substrate impurity concentration," *IEEE Trans. Electron Devices*, vol. 41, no. 12, pp. 2357–2362, Dec. 1994.

[23] J. Mitard, C. Shea, B. De Jaeger, A. Pristera, G. Wang, M. Houssa, G. Eneman, G. Hellings, W.-E. Wang, J. Lin, F. Leys, R. Loo, G. Winderickx, E. Vrancken, A. Stesmans, K. De Meyer, M. Caymax, L. Pantisano, M. Meuris, and M. Heyns, "Impact of EOT scaling down to 0.85 nm on 70 nm Ge-pFETs technology with STI," in *VLSI Symp. Tech. Dig.*, Jun. 2009, pp. 82–83.

[24] C. O. Chui, H. Kim, D. Chi, B. Triplett, P. McIntyre, and K. Saraswat, "A sub-400 °C germanium MOSFET technology with high-κ dielectric and metal gate," in *IEDM Tech. Dig.*, 2002, pp. 437–440.

[25] F. Bellenger, M. Houssa, A. Delabie, V. Afanasiev, T. Conard, M. Caymax, M. Meuris, K. De Meyer, and M. M. Heyns, "Passivation of Ge(100)/ GeO_2/high-kappa gate stacks using thermal oxide treatments," *J. Electrochem. Soc.*, vol. 155, no. 2, pp. G33–G38, 2008.

[26] K. Martens, C. O. Chui, G. Brammertz, B. De Jaeger, D. Kuzum, M. Meuris, M. Heyns, T. Krishnamohan, K. Saraswat, H. Maes, and G. Groeseneken, "On the correct extraction of interface trap density of MOS devices with high-mobility semiconductor substrates," *IEEE Trans. Electron Devices*, vol. 55, no. 2, pp. 547–556, Feb. 2008.

[27] G. Hellings, E. Rosseel, T. Claryssea, D. Petersen, O. Hansen, P. Nielsen, E. Simoen, G. Eneman, B. De Jaeger, T. Hoffmann, K. De Meyer, and W. Vandervorst, "Systematic study of shallow junction formation on germanium substrates," *Microelectron. Eng.*, 2010, to be published.

[28] G. Du, X. Y. Liu, Z. L. Xia, Y. K. Wang, D. Q. Hou, J. F. Kang, and R. Q. Han, "Evaluations of scaling properties for Ge on insulator MOSFETs in nano-scale," *Jpn. J. Appl. Phys.*, vol. 44, no. 4B, pp. 2195–2197, Apr. 2005.

Geert Hellings (S'07) was born in Ukkel, Belgium, on February 22, 1984. He received the M.S. degree in electrical engineering from the University of Leuven, Leuven, Belgium, in 2007, with a thesis on III-nitride-based UV detectors for space applications. He is currently working toward the Ph.D. degree at the University of Leuven and imec, Leuven, on the topic of high-mobility channel materials for digital logic applications.

He receives a Ph.D. grant from the Institute for the Promotion of Innovation through Science and Technology in Flanders (IWT-Vlaanderen), Brussels, Belgium.

Geert Eneman received the B.S. and M.S. degrees in electrical engineering and the Ph.D. degree on the topic of "Design, fabrication, and characterization of strained silicon transistors" from the Catholic University of Leuven, Leuven, Belgium, in 1999, 2002, and 2006, respectively. His Ph.D. work was done in imec, Leuven.

He currently holds a Postdoctoral position at the Catholic University of Leuven. He is also currently with the Department of CMOS Technology, imec. He is a Postdoctoral Fellow with the Fund for Scientific Research-Flanders (FWO-Vlaanderen), Brussels, Belgium. His current research interests include the characterization and modeling of Ge MOS devices, Ge junction analysis, and modeling of alternative device structures.

Raymond Krom received the B.S. and M.S. degrees in microelectronic engineering from the Rochester Institute of Technology, Rochester, NY, in 2005 and 2008, respectively. He is currently working toward the Ph.D. degree in electrical engineering at the Catholic University of Leuven, Leuven, Belgium, and imec, Leuven, on the topic of electrical characterization and carrier transport in germanium devices.

His research interests include service learning in engineering and electrical characterization of high-mobility devices for use in digital logic applications.

Brice De Jaeger received the B.S. and M.S. degrees in electrical engineering from Universiteit Gent, Ghent, Belgium, in 1994 and 1997, respectively.

Since 1997, he has been a Researcher with the Department of CMOS Device Research, imec, Leuven, Belgium. His current research interests include the technology, device integration, and characterization of germanium and III/V transistors.

Jérôme Mitard received the M.S. degree in microelectronic engineering from the Polytechnic University School of Marseille, Marseille, France, in 2003 and the Ph.D. degree in microelectronics from the MINATEC Center, Grenoble, France.

After his Ph.D. degree, he joined imec, Leuven, Belgium, as a Postdoctoral Researcher, where he is currently working on the integration of germanium and II–V substrates for the 22-nm CMOS node. For three years, he acted as an ST Assignee with CEA-LETI, Grenoble, where he was involved in the electrical characterization of hafnium-based dielectrics with metal gate for sub-70-nm CMOS technologies.

An De Keersgieter received the M.S. degree in physics from Ghent University, Ghent, Belgium, in 1984.

She joined imec, Leuven, Belgium, in 1985, working on process modeling. She has been involved in modeling and simulation work for several European projects such as STORM, ADEQUAT, ACE, HUNT, ARTEMIS, NANOCMOS, and PULLNANO. She is currently mainly focusing on process and device simulation and calibration of 65-nm and smaller CMOS technologies. Among her fields of interest are strain engineering and multigate devices. Then, she is responsible for the support of TCAD tools used at imec.

Ms. De Keersgieter is a member of the Scientific Committee (Modeling and Simulation) for the ESSDERC Conference and is also active in the European Modeling and Simulation Technology Working Group of ITRS.

Thomas Hoffmann received the Ph.D. degree from Lille University, Lille, France, in 2000.

He then joined Intel Corporation's R&D Group, Hillsboro, OR, as a TCAD Engineer for sub-90-nm technologies. In 2004, he moved to Intel's Technology Development Group as a Device Engineer for 45-nm process development. In 2005, he joined imec, Leuven, Belgium, to lead the Electrical Characterization Group for advanced silicon technologies. In 2009, he became the Director of the FEOL Logic and DRAM devices research program. He has authored or coauthored approximately 50 technical papers for publication in journals and presentations at conferences.

Marc Meuris received the M.S. and Ph.D. degrees in physics from the Katholieke Universiteit Leuven, Leuven, Belgium, in 1983 and 1990, respectively.

In 1984, he was with imec, Leuven, where, in the first year, he did process the development of RTP anneals of dopants in III–V materials. Then, he transferred to the Analysis Group, imec, headed by W. Vandervorst, where he did his Ph.D. work on secondary ion-mass spectroscopy. From 1990 to 1999, he was with the group of M. Heyns on cleaning technology for improving gate oxide integrity, resulting in the development of the imec Clean as a pregate and prediffusion clean for CMOS processing. From 1997 to 2002, he was the CMP Group Leader with imec. In 2002, he was the Technical Advisor for imec projects in collaboration with the Flemish industry. Since 2003, he has been the Program Manager of the Ge program at imec. In 2006, this program enlarged its focus to Ge and III–V materials for scaling CMOS application. In 2009, he became the III–V Program Manager.

Kristin De Meyer (S'73–M'79–SM'00) received the M.Sc. degree in electrical engineering and the Ph.D. degree from the Katholieke Universiteit Leuven (KUL), Leuven, Belgium, in 1974 and 1979, respectively.

From November 1979 to November 1980, she was granted an IBM World Trade Postdoctoral Fellowship and was with the IBM T. J. Watson Research Center, Yorktown Heights, NY, on the development of EAROMs using Si-rich oxides. At the end of 1980, she returned to KUL as a Senior Research Assistant and, in October 1982, a Research Associate of NFWO. With the foundation of the Interuniversity Microelectronics Center (imec), Leuven, her activities moved from KUL to imec, where she initially remained as a Research Associate of NFWO. Since October 1989, she has been a Regular Employee with imec, where, from 1985 to 1992, she was the Head of the group on process and device modeling and simulation, working on process optimization techniques, parameter extraction, analytical and numerical device modeling, and computational physics. In addition, statistical process control activities were monitored through her group. From January 1993 to December 2002, she was in charge of deep-submicrometer MOS technology and exploratory field-effect devices. In January 2003, she became the Strategic Coordinator of Doctoral Research with imec. Since October 1986, she has also been a part-time Professor with ESAT-INSYS, KUL. She was the Coordinator for imec in the ESPRIT 962 EVEREST, STORM, NOVA, ULTRA, VAHMOS2000 (prime), FASEM, and ULIS projects; in the IST SIGMUND (prime), SATURN (SOI), and NESTOR projects; and in the Marie Curie EST EDITH project. She was also involved in the ESPRIT ACCESS program, ADEQUAT, ACE, and IST HUNT. She also managed the HCM-SUSTAIN network on deep-submicrometer silicon technology with 21 partners from academia and research institutes. She authored or coauthored over 300 publications and organized summer courses, the SISPAD '98 Conference, and the ULIS 2004 Workshop.

Dr. De Meyer is a member of the Flemish and the Belgian Federal Council for Science Policy. She is currently the Editor for the IEEE ELECTRON DEVICE LETTERS and a member of the ITRS working groups on process integration, devices and structures, and emerging research devices.